This document is a part of Main Course File			Document No.: CFM – 8		
This document is a		SARDAR VALLABHBHAI PATEL EDUCATION SOCIETY MANAGED N. G. PATEL POLYTECHNIC ELECTRICAL ENGINEERINNG DEPARTMENT ASSIGNMENTS			
Semester / Year: Second/ First					
Assignment Number: 1					
Assignment CO Number: DI02000161.1					
Sr. No.	Questions related to Course Outcomes				
Part – A	Questions carrying 3 Marks				
1	Perform binary subtractions: $(11010111.1110)_2 - (11101111.01110)_2 = (20)_2 = (20)_3 = (20)_{10} = $				
Part – B	Questions carrying 4 Marks				
1	Explain weig	Explain weighted & non weighted code with suitable example.			
Part – C	Questions carrying 7 Marks				
1	Using 2's compliment method, perform binary subtraction. Subtract also using direct Method & check the results. (110011001101)2 –(010111110)2				
Mr. Nirav C. PandyaMr.Nilesh P.PrajapatiPrepared By: (Name of Faculty (ies)) withSignature of Head of DepartmentsignatureSignature					

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		<b>N. G. PATEL POLYTECHNIC</b>				
ISROLI-AFWA		ELECTRICAL ENGINEERINNG DEPARTMENT				
ASSIGNMENTS						
Course Na	ame (With Co	de): Fundamentals of Digital	Electronics (DI02000161)			
Semester /	/ Year: Secon	d/ First				
Assignme	nt Number: 2					
Assignme	nt CO Numbe	er: DI02000161.2				
Sr. No.	Questions related to Course Outcomes					
Part – A	Questions carrying 3 Marks					
1	1. Explain different types of logic gate with truth table & symbol.					
-	2.  A+A'B=A+B					
Part – B	Questions carrying 4 Marks					
1	1. Prove NAND gate as universal gate with logic circuit & truth table.					
	2. Expla	2. Explain De-Morgan's theorem in detail with logic circuit & truth table.				
Part – C	Questions carrying 7 Marks					
	1. $A+BC=(A+B)(A+C)$					
1	2. $(AB+BC+CA)^2 = A^2B^2+B^2C^2+C^2A^2$					
	3. Solve the example: AB+A'B+AB'					
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19 ISR	ELECTRICAL	ELECTRICAL ENGINEERINNG DEPARTMENT			
ASSIGNMENTS					
Course Name (With Code): Fundamentals of Digital Electronics (DI02000161)					
Semester /	/ Year: Second/ First				
Assignme	nt Number: 3				
Assignment CO Number: DI02000161.3					
Sr. No.	Questions related to Course Outcomes				
Part – A	Questions carrying 3 Marks				
1	1. Define following term : SOP,POS	, Min term, Max Term			
1	2. Why K- map is use? What is don't care condition?				
Part – B	Questions carrying 4 Marks				
1	1. Draw basic construction of 2, 3 & 4 variable K- map.				
1	2. Solve $f(A,B,C) = \sum m(0,1,4,5,6,7)$				
Part – C	Questions carrying 7 Marks				
	1. $f(A,B,C,D) = \sum m(0, 1, 4, 5, 14, 15) + d(10,11)$ and implement it by using NAND				
1	gate only.				
	2. $f(A,B,C,D) = \pi m(0, 1, 4, 5, 14, 15) + d(10,11)$ and implement it by using NOR gate				
	only.				
	1 4				
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STEL REAL		MANAGED		
		N. G. PATEL POLYTECHNIC		
ISROLI-AFWA		ELECTRICAL ENGINEERINNG DEPARTMENT		
		ASSIGNMENTS		
Course Name (With Code): Fundamentals of Digital Electronics (DI02000161)				
Semester / Year: Second/ First				
Assignment Number: 4				
Assignment CO Number: DI02000161.4				
Sr. No.	Questions related to Course Outcomes			
Part – A	Questions carrying 3 Marks			
1	1. Expla	ain 8:1 Mux in brief.		
-	2. Expla	in 1:4 De-mux in brief.		
Part – B	Questions ca	Questions carrying 4 Marks		
1	1. Expla	1. Explain 3 to 8 line decoder in detail.		
-	2. Explain Half Subtractor in detail.			
Part – C	Questions carrying 7 Marks			
1	1. Explain Full Subtractor with logic circuit, logic equation & truth table.			
-	2. Explain Full Adder with logic circuit, logic equation & truth table.			
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	CLI-AFWA ELECTRICAL	ELECTRICAL ENGINEERINNG DEPARTMENT	
	ASSIGN	MENTS	
Course Na	me (With Code): Fundamentals of Digita	ll Electronics (DI02000161)	
Semester /	Year: Second/ First		
Assignmen	nt Number: 5		
Assignmen	nt CO Number: DI02000161.5		
Sr. No.	Questions related to Course Outcomes		
Part – A	Questions carrying 3 Marks		
1	1 1. Define Flip flop. Explain SR flip flop with truth table.		
Part _ R	2. Explain Clock KS hip hop. Questions corrying 4 Marks		
	1 Compare Combinational & Sequential circuits		
1	2. Explain D & T Flip flop with circu	with circuit & truth table.	
Part – C	Ouestions carrying 7 Marks		
1	<ol> <li>What is race around condition? Explain JK flip flop in detail.</li> <li>Short note on Master Slave JK flip flop.</li> </ol>		
	Mr. Nirav C. Pandya	Mr.Nilesh P.Prajapati	
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