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SARDAR VALLABHBHAI PATEL EDUCATION SOCIETY MANAGED

N. G. PATEL POLYTECHNIC

COMPUTER ENGINNEERING DEPARTMENT

FORMAT FOR ASSIGNMENTS

Course Name (With Code): Computer Organization & Architecture (4350701)

Semester / Year: Fifth / Third

Assignment Number: 1

Assignment CO Number: 4350701.1

Sr. No.	Questions related to Course Outcomes
Part – A	**Questions carrying 3 Marks**
1	Define Processor
2	Advantages and disadvantages of serial bus
3	Advantages and disadvantages of parallel bus
4	
5	
Part – B	**Questions carrying 4 Marks**
1	Draw neat sketch of block diagram of digital computer
2	Explain all register in detail(PC,IR,SP,MAR,MDR,ACCUMLATOE etc.)
3	Compare serial and parallel bus
4	
5	
Part – C	**Questions carrying 7 Marks**
1	Classify characteristics of Intel processor
2	Explian characteristics of intel processor from 4bit (40004) to i7
3	Explain shared bus in brief
4	Explain dedicated bus in detail
5	

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FORMAT FOR ASSIGNMENTS

Course Name (With Code): Computer Organization & Architecture (4350701)

Semester / Year: Fifth / Third

Assignment Number: 2

Assignment CO Number: 4350701.2

Sr. No.	Questions related to Course Outcomes
Part – A	**Questions carrying 3 Marks**
1	Draw pin diagram of 8085 microprocessor.
2	Explain function of each pin of 8085 microprocessor.
Part – B	**Questions carrying 4 Marks**
1	Explain flag register of 8085 microprocessor.
2	Explain 8085 bus organization in brief.
Part – C	**Questions carrying 7 Marks**
1	Explain architecture of 8085 microprocessor with neat diagram.

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FORMAT FOR ASSIGNMENTS

Course Name (With Code): Computer Organization & Architecture (4350701)

Semester / Year: Fifth / Third

Assignment Number: 3

Assignment CO Number: 4350701.3

Sr. No.	Questions related to Course Outcomes
Part – A	**Questions carrying 3 Marks**
1	Give classification of interrupt with its priority. Explain each in short.
2	Define machine cycle, T state, OPCODE, OPERAND.
3	Write a program to sum integer from 0 to 9. Store result in register L.
Part – B	**Questions carrying 4 Marks**
1	List addressing modes of 8085 microprocessor. Explain each with suitable example.
2	Give classification of instruction & explain each with suitable example.
3	Write a program to find maximum number from block of number store in memory location.
Part – C	**Questions carrying 7 Marks**
4	Write a program to add 2034H & 5645H. store result in register pair HL.
5	Explain any 4 arithmetic & logical instruction with byte, addressing modes & function.
3	Explain following instructions: LDA C200H, LXI B, D600H, DAA, PUSH PSW, RLC, CMP M, INX H.

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FORMAT FOR ASSIGNMENTS

Course Name (With Code): Computer Organization & Architecture (4350701)

Semester / Year: Fifth / Third

Assignment Number: 4

Assignment CO Number: 4350701.4

Sr. No.	Questions related to Course Outcomes
Part – A	**Questions carrying 3 Marks**
1	Compare primary memory and secondary memory
2	Explain ROM
3	Explain RAM
4	Difference between SRAM and DRAM
Part – B	**Questions carrying 4 Marks**
1	Explain DMA
2	Explain associative mapping scheme
3	Write a short note on Memory classification
4	Explain memory Hierarchy
5	Draw and explain 4 level of memory
Part – C	**Questions carrying 7 Marks**
1	Explain working of associative memory
2	Explain magnetic disk storage media
3	Explain RAM,ROM,PROM,EPROM
4	Compare ROM and RAM
5	Explain secondary memory in detail
6	Write short note on Mapping scheme
7	Write short note on cache memory
8	Write short note on virtual memory

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FORMAT FOR ASSIGNMENTS

Course Name (With Code): Computer Organization & Architecture (4350701)

Semester / Year: Fifth / Third

Assignment Number: 5

Assignment CO Number: 4350701.5

Sr. No.	Questions related to Course Outcomes
Part – A	**Questions carrying 3 Marks**
1	Explain peripheral devices in detail
2	Define I/O interface
3	Explain Program I/O
Part – B	**Questions carrying 4 Marks**
1	Explain I/O interface unit in detail
2	explain I/O interface with example
3	Describe IOP
Part – C	**Questions carrying 7 Marks**
1	List out different mode of data transfer with I/O
2	Explain interrupt initiated I/O transfer
3	Describe input output processor in detail
4	Explain CPU/IOP communication with block daigram

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